Key Challenges of Dry Etching Technology for Beyond 20nm Semiconductor Device Era

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Recent boom-up of smart devices and further usage of semiconductor chips for automobiles and medical equipments, etc will keep motivating the development of semiconductor industry. Semiconductor devices fabrications have met many new circumstances regarding the future development directions. First, DRAM (Dynamic Random Access Memory) is the in the stage of sub 20nm design rule development in an R&D level. Second, NAND flash development has two directions. One is to extend the shrinkage of planar flash already in the sub 20nm age. The other strategy is to change the paradigm of flash memory fabrication by introducing VNAND (Vertical-NAND) In addition, logic devices also have been experiencing many challenges while developing devices such as L20, L14, and L10, etc.

Dry etching technology, which is a core part of semiconductor device fabrication, cannot avoid many difficulties to cope with above challenging situation changes. (1) Unsatisfactory development speed of EUV lithography for the last several years has made DPT (Double Patterning Technology) and QPT (Quadruple Patterning Technology) more necessary for sub 20nm devices development. It means that global and local CD (Critical Dimension) distribution control should be very tight because even 1nm shift during the unit step can amplify variation during DPT and QPT. (2) There has been tremendous increase of difficulties for HARC (High Aspect Ratio Contact) etching. DRAM capacitor mold etching, VNAND channel hole etching, MC (Metal Contact etching are typical examples. (3) Wafer-to-wafer, lot-to-lot, and tool-to-tool process variation management will be more demanding. (4) New material/new structure introduction does seriously request etch engineers to do an innovative approach for achieving goals. Some new memories such as FeRAM, PC-RAM, and M-RAM are typical examples. As a good example, MRAM MTJ (magnetic tunnel junction) materials have several noble nonvolatile metals. It is quite difficult to etch the material without sidewall redeposition. We need to seek better understanding and general insights for future technology developments.

In this work, I will mention future etching technology development directions to tackle the above challenges.